

IN THE CLAIMS:

Sub B2
1 (currently amended)

2 A backplane system to connect in common a plurality
3 of peripheral computing devices each on an individual daughter card such that
4 there is a corresponding number of daughter cards, wherein the daughter cards
5 are configured as cPCI-compliant cards each having a slot connector, the back-
6 plane system comprising:

- 7 a. a backplane bus having a plurality of slots for receiving one or more
8 of the cPCI-compliant cards, wherein said slots are spaced from one
9 another at a pitch to minimize impedance mismatching, each slot in-
10 cluding a card connector; and
11 b. an interposer card for each daughter card, said interposer card in-
12 cluding means to connect to the slot connector and to said card
13 connector such that said interposer card is interposed between the
14 daughter card and a slot of said plurality of slots of said backplane
15 bus, wherein said interposer card is constructed to reduce the re-
16 fective wave path from the daughter card to the interposer card,
17 thereby reducing the impedance mismatch and thereby allowing
18 the noise to settle in time for the interposer card to output, in re-
19 sponse to receiving a reflective wave, an incident wave is designed
20 to convert reflective wave of the daughter card into incident wave
switching at said slot connector.

1 2. (original) The backplane system as claimed in **Claim 1** wherein said back-
2 plane bus is a cPCI backplane, the system further comprising a cPCI interface
3 coupled between said backplane bus and the daughter cards, wherein said inter-
4 poser card is couplable between said cPCI interface and said slot connector of
5 said backplane bus.

1 3.(original). The backplane system as claimed in **Claim 2** wherein said cPCI
2 interface includes a state machine to regulate timing, direction and enablement
3 associated with operation of said interposer card.

1 4.(original). The backplane system as claimed in **Claim 3** wherein said state
2 machine and said interposer card are implemented integrally with said interface.

1 5.(original). The backplane system as claimed in **Claim 1** wherein said interposer
2 card includes a GTLP transceiver to produce incident wave switching.

1 6.(original). The backplane system as claimed in **Claim 1** wherein said back-
2 plane bus has an impedance of about 65 ohms.

1 7.(original). The backplane system as claimed in **Claim 1** wherein said back-
2 plane bus further includes impedance terminations at opposing ends thereof.

1 8.(original). The backplane system as claimed in **Claim 7** wherein each of said
2 impedance terminations of said backplane has an impedance of about 40 ohms.

1 9.(original). The backplane system as claimed in **Claim 1** wherein each of said
2 slots includes a stub connector having a stub impedance of about 50 ohms.

1 10.(original) The backplane system as claimed in **Claim 1** wherein said back-
2 plane bus includes 21 of said plurality of slots.

1 11.(currently amended) A method of increasing the throughput of a conven-
2 tional cPCI-compliant backplane architecture having a plurality of slots coupled to
3 a common backplane bus for receiving one or more cPCI-compliant daughter cards,
4 the method comprising the step of inserting an interposer card between each of

5 the daughter cards and its corresponding slot, wherein said interposer card in-
6 cludes means for reducing the reflective wave path from the daughter card to the
7 interposer card, thereby reducing the impedance mismatch and thereby allowing
8 the noise to settle in time for the interpose card to output, in response to receiv-
9 ing a reflective wave, an incident wave, converting reflective-wave switching as-
10 sociated with signal propagation of the daughter card into incident-wave switching
11 at the backplane bus.

1 12.(original). The method as claimed in **Claim 11** further comprising the step of
2 installing at the ends of the backplane bus termination impedances each having
3 an 30 impedance of about 40 ohms.

1 13.(original). The methol as claimed in **Claim 11** further comprising the step of
2 forming stub connectors of each of the slots with stub impedances of about 50 ohms.

1 14.(original). The method as claimed in **Claim 11** further comprising the step of
2 coupling said interposer card with a state machine configured to regulate timing,
3 direction, and enablement of said incident-wave switching.

1 15.(original). The method as claimed in **Claim 11** wherein said interposer card
2 includes a GTLP transceiver for generating said incident-wave switching.

1 16.(original). The method as claimed in **Claim 11** wherein said backplane bus
2 has an impedance of about 65 ohms.

1 17.(original). The method as claimed in **Claim 11** further comprising the step of
2 latching the signal transmissions associated with said incident-wave switching so
3 as to control the signal propagation to and from the backplane bus.

1 18.(original). The method as claimed in **Claim 11** wherein the backplane bus is a
2 cPCI backplane and one or more of the daughter cards is a cPCI-compliant card, further
3 comprising the step of interposing between the cPCI-compliant card and the inter-
4 poser card a cPCI interface.

1 19.(original). The method as claimed in **Claim 18** further comprising a state ma-
2 chine formed integrally with said interface, wherein said state machine regulates
3 operation of said interposer card.

1 20.(original). The method as claimed in **Claim 18** further comprising a state machine
2 formed integrally with said interface, wherein said state machine regulates operation of
3 said interposer card, further comprising the step of forming said interposer card inte-
4 grally with said interface.